AMENDMENTS

Please amend the claims as follows:

1. (Currently Amended) A crossbar device comprising:

n input lines;

m output lines; and

a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to selectively couple said n input lines to said m output lines, wherein at least one of the plurality of chains of pass transistors comprises a first and a second pass transistor coupled such that said first transistor drives a load consisting essentially of said second transistor and interconnect between said first and said second transistor;

where n and m are integers.

2. Please cancel claim 2.

3. (Previously Amended) The crossbar device of claim 1, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

4. (Original) The crossbar device of claim 1, wherein the device further comprises a plurality of memory elements coupled to the input lines.

5. (Previously Amended) The crossbar device of claim 1, wherein the device further comprises a plurality of p to q decoder logics coupled to the input lines, where p and q are integers, with p being less than q.

6. (Original) The crossbar device of claim 1, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

7. (Currently Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically associated with ~~the memory element~~said at least a memory element; and

a voltage supply structure coupled to ~~the~~ at least one crossbar device designed to supply Vdd to an input to the output buffer~~s~~, and a voltage raised by a threshold over Vdd to ~~the memory element~~said at least a memory element to maintain ~~the~~ an input voltage of the output buffer~~s~~ at Vdd.

8. (Previously Amended) The reconfigurable circuit of claim 7, wherein at least one of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

9. (Previously Amended) The reconfigurable circuit of claim 8, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transistor.

10. (Previously Amended) The reconfigurable circuit of claim 8, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

11. (Previously Amended) The reconfigurable circuit of claim 7, wherein each of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

12. (Previously Amended) The reconfigurable circuit of claim 11, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

13. (Original) The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is an integrated circuit.

14. (Original) The reconfigurable circuit of claim 7, wherein the reconfigurable circuit is a block of an integrated circuit.

15. (Currently Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and

a power-on circuitry coupled to the crossbar devices to force the output buffers to a same known logic value at power-on, said same known logic value to facilitate reduction of current drain in said reconfigurable circuit by reducing ~~contention~~ the number ~~on~~ of outputs of said plurality of output buffers at different logic values.

16. (Original) The reconfigurable circuit of claim 15, wherein the power-on circuitry comprises a flip-flop.

17. (Previously Amended) The reconfigurable circuit of claim 15, wherein at least one of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

18. (Previously Amended) The reconfigurable circuit of claim 17, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass transistor.

19. (Previously Amended) The reconfigurable circuit of claim 17, wherein each of the plurality of chains of pass transistors consists of a first and a second pass transistor.

20. (Previously Amended) The reconfigurable circuit of claim 15, wherein each of the plurality of crossbar devices comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

21. (Original) The crossbar device of claim 20, wherein each of said chains of pass transistors further comprises a memory element coupled to a pass transistor of the chain, disposed on an input side of the chain to control the chain.

22. (Previously Amended) The reconfigurable circuit of claim 15, wherein

each crossbar device further having at least a memory element electrically associated to an output buffer; and

the reconfigurable circuit further comprises a voltage supply structure coupled to the crossbar devices designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the voltage supply of the output buffers at Vdd.

23. (Original) The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is an integrated circuit.

24. (Original) The reconfigurable circuit of claim 15, wherein the reconfigurable circuit is a block of an integrated circuit.

25. (Previously Presented) The reconfigurable logic circuit of claim 7 wherein provision of Vdd at the input voltage of the output buffer is to facilitate reduction of parasitic current flow through a first inversion stage.

26. (New) The reconfigurable circuit of claim 15, wherein the same known logic value is a logic "0".